What is claimed is:

1. An apparatus, comprising:

an edge detector, the edge detector configured to receive an input signal and a counter signal, the edge detector further configured to send a plurality of time values based on the input signal and the counter signal, each time value from the plurality of time values being uniquely associated with a detected edge transition from the input signal;

a memory coupled to the edge detector, the memory configured to receive from the edge detector the plurality of time values, the memory being configured to store the plurality of time values; and

a pulse-input engine coupled to the memory, the pulse-input engine configured to measure a plurality of pulse-to-pulse delays based on the plurality of time values stored in the memory.

2. The apparatus of claim 1, wherein:

the pulse-input engine is configured to measure the plurality of pulse-to-pulse delays on a per-pulse basis when a prior pulse-to-pulse delay is below a predefined threshold; and

the pulse-input engine is configured to measure the plurality of pulse-to-pulse delays over a plurality of pulses when a prior pulse-to-pulse delay exceeds the predefined threshold.

3. The apparatus of claim 1, wherein:

the input signal corresponds to a signal associated with a rotating gear having a plurality of gear teeth, each gear tooth from the plurality of gear teeth corresponding to an edge transition from the input signal.

4. The apparatus of claim 1, wherein:

the edge detector further includes an input filter, the input filter includes a valid-data counter and a threshold selector, the input filter is configured to provide a valid indication when the valid-data counter exceeds a predetermined threshold, the threshold selector of the input filter is configured to select the predetermined threshold based on an input frequency associated with the input signal.

5. The apparatus of claim 1, further comprising:

a zero-speed tester coupled to the edge detector and the pulse-input engine, the zero-speed tester being configured to receive a test signal from the edge detector and to send a test-pulse signal to a comparator coupled to the edge detector,

the edge detector configured to send the test signal to the zero-speed tester when the edge detector measures a frequency of the input signal below a predetermined threshold.

6. The apparatus of claim 1, wherein the pulse-input engine is configured to check for an interval time between pulses from the input signal on a per-pulse basis, the pulse-input engine is configured to send a missing-pulse indication if the interval time exceeds a predetermined threshold, the predetermined threshold being based on a frequency of the input signal.

7. The apparatus of claim 1, wherein the edge detector further includes:

an adaptive debounce filter having an associated debounce filter length greater than a length of a spurious edge transition, the adaptive debounce filter configured to adjust the associated debounce filter length based on a frequency of the input signal.

8. The apparatus of claim 1, wherein:

the memory includes an input port and an output port, the input port of the memory being coupled to the edge detector, the output port of the memory being coupled to the pulse-input engine, the memory configured to store the time value for each detected edge transition in a circular manner.

9. The apparatus of claim 1, wherein the input signal has a plurality of pulses having a frequency between substantially 0.5 Hz and 32,000 Hz.

10. The apparatus of claim 1, further comprising:

a second edge detector, the second edge detector configured to receive the signal and the clocked-timer signal, the second edge detector further configured to send its own time value for each detected edge transition from the input signal;

a second memory coupled to the second edge detector, the second memory configured to receive from the second edge detector its own time value for each detected edge transition from the input signal, the second memory being configured to store the time value for each detected edge transition for the second edge detector;

a second pulse-input engine coupled to the second memory, the second pulse-input engine configured to measure a pulse rate based on the time value for each detected edge transition stored in the second memory;

a third edge detector, the third edge detector configured to receive the signal and the clocked-timer signal, the third edge detector further configured to send its own time value for each detected edge transition from the input signal;

a third memory coupled to the third edge detector, the third memory configured to receive from the third edge detector its own time value for each detected edge transition from the input signal, the third memory being configured to store the time value for each detected edge transition for the third edge detector; and

a third pulse-input engine coupled to the third memory, the third pulse-input engine configured to measure a pulse rate based on the time value for each detected edge transition stored in the third memory.

11. The apparatus of claim 10, further comprising:

a first processor coupled to the pulse-input engine, the first processor calculating a pulse rate based on the pulse-to-pulse delay from the pulse-input engine;

a second processor coupled to the second pulse-input engine and the first processor, the second processor calculating a pulse rate based on the pulse-to-pulse delay from the second pulse-input engine; and

a third processor coupled to the third pulse-input engine, the first processor and the second processor, the third processor calculating a pulse rate based on the third pulse-to-pulse delay from the pulse-input engine,

the first processor, second processor and the third processor calculating a voted pulse rate based on the pulse rate calculated by the first processor, the pulse rate calculated by the second processor, and the pulse rate calculated by the third processor.

12. The apparatus of claim 1, further comprising:

an input device coupled to the pulse-input engine, the input device configured to receive a sensor-type indicator, a gear-teeth-number indicator, an edge-type indicator and an active-sensor field-voltage indicator.

13. A method for determining a revolution rate for a gear, comprising:

performing the following steps for each of at least three subsystems operating in parallel:

detecting a plurality of edge transitions within a input signal based on a counter signal;

storing a time value for each edge transition from the plurality of edge transitions; and

calculating a plurality of pulse-to-pulse delays based on the time value for each edge transition from the plurality of edge transitions.

14. The method of claim 13, wherein:

the each pulse-to-pulse delay from the plurality of pulse-to-pulse delays is calculated on a per-pulse basis when a prior pulse-to-pulse delay is below a predefined threshold; and

the each pulse-to-pulse delay from the plurality of pulse-to-pulse delays is calculated over a plurality of pulses when a prior pulse-to-pulse delay exceeds the predefined threshold.

15. The method of claim 13, wherein each subsystem further performs:

measuring an interval time between a first edge transition and a second edge transition from the plurality of edge transitions; and

sending a missing-pulse indication if the interval time exceeds a predetermined threshold.

16. The method of claim 13, wherein each subsystem further performs:

detecting a test signal having a frequency below a predetermined frequency;

sending a zero-speed test pulse to a front-end comparator when the test signal is detected; and

suspending the storing step for the zero-speed test pulse when the test signal is detected.

17. The method of claim 13, wherein each subsystem further performs:

measuring an interval time between a first edge transition and a second edge transition from the plurality of edge transitions; and

filtering the first edge transition when the interval time is below a predetermined threshold, the predetermined threshold being based on a frequency of the input signal.

18. The method of claim 13, further comprising:

receiving a sensor-type indicator, a gear-teeth-number indicator and an edge-type indicator;

the calculating of the plurality of pulse-to-pulse delays being based on the sensor-type indicator, the gear-teeth-number indicator and the edge-type indicator.

19. The method of claim 18, further comprising:

receiving a field-voltage indicator when the sensor-type indicator indicates an active sensor.

20. An apparatus, comprising:

a pulse-input measurement system having at least three redundant subsystems, each subsystem having:

an input filter network configured to receive an input signal to produce a filtered signal;

a comparator coupled to the input filter network, the comparator configured to receive the filtered signal and to produce a comparator signal; and

an input-output controller coupled to the comparator, the input-output controller configured to receive the comparator signal and to produce a pulse-to-pulse delay value.

21. The apparatus of claim 20, wherein the at least three redundant subsystems each include:

an isolated bus transceiver coupled to the pulse-input module for that redundant subsystem, the isolated bus transceiver configured to receive the pulse-rate value and send an output signal for that redundant subsystem.

22. The apparatus of claim 20, further comprising:

at least three input/output buses each being uniquely coupled to the input-output controller of the at least three redundant subsystems of the pulse-input measurement system,

each input/output bus being configured to receive the pulse-to-pulse delay value from the respective redundant subsystem of the pulse-input measurement system; and

at least three processors each being uniquely coupled to the at least three input/output buses, the at least three processors configured to receive the pulse-to-pulse delay value from the respective input/output bus, the at least three processors configured to send an optimal pulse-rate value based on the pulse-to-pulse delay value associated with each redundant subsystem.

23. The apparatus of claim 22, wherein the at least three processors are configured to calculate the optimal pulse-rate value by selecting a median of the pulse-rate value from each subsystem of the pulse-input measurement system when each pulse-rate value from each subsystem of the pulse-input measurement system has a non-zero value.

24. The apparatus of claim 22, wherein the at least three processors are configured to calculate the optimal pulse-rate value by averaging the pulse-rate value from each subsystem of the pulse-input measurement system when the pulse-rate value for one subsystem of the pulse-input measurement system has a zero value.

25. The apparatus of claim 22, wherein the at least three processors are configured to select the pulse-rate value from one redundant subsystem as the optimal pulse-rate value when the pulse-rate value for one redundant subsystem has a zero value, the selected pulse-rate value being a highest value.

26. The apparatus of claim 22, wherein, when the pulse-rate value for one redundant subsystem has a zero value, the at least three processors are configured to calculate the optimal pulse-rate value by averaging the pulse-rate from the remaining redundant subsystems from the at least three redundant subsystems.

27. The apparatus of claim 22, wherein the at least three processors are configured to select the pulse-rate value from one redundant subsystem as the optimal pulse-rate value, when the pulse-rate value for that one redundant subsystem has a non-zero value and the pulse-rate values for the remaining redundant subsystems have a zero value.

28. The apparatus of claim 20, wherein the comparator of each subsystem includes complimentary hysteresis portions.